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EXAMINER	
PAPPAS, PETER	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,953	SEILER ET AL.	
	Examiner	Art Unit	
	PETER-ANTHONY PAPPAS	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-15,19 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 23-25* is/are allowed.

6)☒ Claim(s) *1-11,13-15 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 19 and 23-25 are allowed. In regard to said claims the cited prior art of record fails to teach or suggest the respective claim limitations when considered as a whole, specifically: wherein the hierarchical Z buffer and stencil cache provides a cache MinZ, cache MaxZ, and a stencil code specifying whether stencil values in the tile are at least equal to, less than or greater than a background stencil value upon which the tile is being compared to the comparator.

2. Claims 1-7 and 26-31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 set forth in this Office action.

3. Claims 14 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim Objections

4. Claims 19, 24 and 25 are objected to because of the following informalities: lack of antecedent basis. Said claims disclose "The apparatus of claim 23." However claim 23 discloses "A graphics processing engine." Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-11, 13-15, 26 and 27-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Said claims fail to fall

within one of the four statutory categories of invention. Supreme Court precedent[1] and recent Federal Circuit decisions[2] indicate that a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process. For example, a process for hierarchical Z buffering and stenciling comprising [1] comparing, updating and determining steps, [2] receiving, determining and updating steps or [3] determining steps is of sufficient breadth that it would be reasonably interpreted as a series of steps completely performed mentally, verbally or without a machine.

It is noted that said claims disclose a "graphics processing engine." However, it is noted that said "graphics processing engine" is merely disclosed in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Furthermore, the respective claim language fails to disclose what exactly

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[1] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

[2] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

constitutes a "graphics processing engine." Assuming arguendo that said "graphics processing engine" defines some type of structure for performing said method it is noted that "the mere use of the machine to collect data necessary for application of the mental process may not make the claim patentable subject matter." Comiskey, 499 F.3d at 1380 (citing In re Grams, 888 F.2d 835, 839-40 (Fed. Cir. 1989)). In other words, nominal or token recitations of structure in a method claim should not convert an otherwise ineligible claim into an eligible one.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aila et al. (U.S. Pub. No. US 2005/0134588 A1) in view of Greene et al. (U.S. Patent No. 5, 579, 455).

9. In regard to claim 8 Aila et al. teach: receiving a tile having a plurality of pixels ("…each tile formed of a set of pixels…" – p. 2, ¶ 19; "When images are processed, the frame buffer … containing pixels of an image is typically divided into sets of pixels often called tiles ... The size of the tiles may vary…" – pp. 3-4, ¶ 52; Fig. 4); determining if the tile is visible relative to a stencil (e.g., shadow information; "…Two different categories of shadow polygons remain: shadow polygons that are completely hidden behind the previously rendered geometry and shadow polygons that intersect with the tile volume

of a tile." – p. 4, ¶ 56; "…If the tile volume is not intersected by a shadow polygon, the tile is either fully lit or fully in shadow with respect to the shadow volume defined by the shadow polygons … These tiles are referred to as potential boundary tiles." – p. 4, ¶ 57; "For non-boundary tiles, which are either fully lit or fully in shadow, it is sufficient to carry out the shadow volume algorithm for one point inside the tile or on the edges of the tile. The result of this point applies to the whole tile. If the point is lit, the tile is fully lit. If the point is in shadow, the tile is fully in shadow…" – p. 4, ¶ 60; Fig. 4).

However, Aila et al. fail to teach determining if the tile is visible in a hierarchical Z plane. Greene et al. teach comparing a Z value range of a tile with a hierarchical Z value range comprised of a plurality of Z planes (Abstract; "…the technique augments traditional Z-buffer scan conversion with an image-space Z-pyramid that allows the algorithm to reject hidden geometry very quickly…" – col. 3, ll. 56-64; "…When the basic test fails to show that a polygon is hidden, we go to the next finer level in the pyramid where the previous pyramid region has been divided into four quadrants. Here we attempt to prove that the polygon is hidden in each of the quadrants it intersects. For each of these quadrants, we compare the nearest Z value of the primitive to the value in the Z-pyramid. If the Z-pyramid value is closer, we know the primitive is hidden in the quadrant. If we fail to prove that the primitive is hidden in one of the quadrants, we go to the next finer level of the pyramid for that quadrant and try again. Ultimately, we either prove that the entire polygon is hidden, or we recurse down to the finest level of the pyramid … This recursire test culls a substantial fraction of the hidden primitives in an efficient manner." – col. 6, ll. 9-36; col. 10, ll. 8-67; col. 11, ll. 1-3; "…it will be seen

that it may be desirable to include not only Z-max elements in a depth buffer such as 502, but also Z-min elements. That is, each of the depth elements 512 can contain not only a Z-max element having the farthest depth of any display cell covered by the depth element 512, but also a Z-min element containing the nearest depth value of any of the display cells 204 covered by the depth element 512." – col. 11, ll. 4-12; "The Build Depth Buffer step 719 ... Within each level, an inner iteration is performed to visit each of the depth elements (Z-max elements) in that level. For each such Z-max element, the depth value which is written into that element is the farthest depth value in any of the Z-max elements which are covered by such Z-max element in the next finer granularity level. If the depth buffer 502 also includes Z-min elements, then the inner iteration also visits each of the Z-min elements in the current level. For each such Z-min element, the depth value which is written into that element is the nearest depth value in any of the Z-min elements which are covered by such Z-min element in the next finer granularity level…" – col. 14, ll. 48-67, and col. 15, ll. 1-6; col. 17, ll. 24-40). It is noted that said Z-pyramid is considered to read on hierarchical Z value range (e.g., hierarchical Z buffer). It is noted that the respective Z-min and Z-max values for each depth element within a given granularity level (e.g., tile) are considered to read on a tile Z value range.

It would have been obvious to one skilled in the art, at the time of the Applicant's invention, to incorporate the teachings of Greene et al. into the method taught by Aila et al., because such incorporation, as taught by Greene et al., would allow for the quicker rejection of hidden geometry ("…hierarchical data structures make it possible to reject

hidden geometry very rapidly while rendering visible geometry with the speed of scan conversion…" – Abstract) and would not prove difficult to implement ("…The technique is not difficult to implement…" – col. 4, ll. 2-4) resulting in a more efficient system. Furthermore, Aila et al. teach the use of a rasterizer (e.g., rasterizer 514) for converting a polygon into pixels or samples inside the polygon (p. 5, ¶ 69). Greene et al. teach a means of accelerating scan conversion ("…The method uses … in order to accelerate scan conversion…" – Abstract). It is noted that scan conversion is considered an element of rasterization and thus through such incorporation it would provide a means of processing a greater amount of information in less amount of time resulting in improved efficiency.

It is noted that the respective claim language fails to disclose what exactly constitutes "updating" a hierarchical Z value range or a stencil code. Thus, "updating" is considered to read on "changing." In light of said incorporation it is implicitly taught that during the processing of a tile or group of tiles that respective information retrieved to process said tile(s) (e.g., depth information, shadow/stencil information, etc.) is changed according to the tile(s) accessed as all tiles are not subject to the exact same conditions. For example, for a given tile there may exist a shadow polygon in front of said tile and another shadow polygon completely behind said tile, resulting in said tile being in shadow, while for another tile the same conditions do not apply and said tile is full lit (Aila et al., p. 4, ¶ 59).

It is noted that the respective claim language fails to disclose what exactly constitutes a "background value" or a "stencil value." Aila et al. teach the use of a

multiple-bit indicator for said stencil code ("…the shadow volume rasterization uses only a small subset of the 8-bit stencil buffer values … a four bit stencil value is used…" – pp. 8, 9, ¶s 101, 102), which specifies a relation of all stencil values in the tile relative to a background value ("…it is sufficient to carry out the shadow volume algorithm for one point inside the tile or on the edges of the tile. The result of this point applies to the whole tile." – p. 4, ¶ 60; "…the contribution of the light source is accumulated into the frame buffer by rendering the shadow mask from the stencil buffer…" – p. 7, ¶ 92; "In connection with Fig. 6 entries for storing stencil values (or, more generally, shadow information) were discussed … tile-specific entries of a stencil buffer (or other information store) may be implemented as a combination of a Boolean value and a stencil value…" – p. 8, ¶ 99). It is noted that a "background value" is considered to read on shadow information which affects how a give pixel or pixels are rendered visually.

10. In regard to claim 9 Aila et al. teach generating an indicator (e.g., Boolean boundary value) to indicate whether to render the plurality of pixels within the tile ("If the Boolean boundary value in the temporary tile classification buffer is TRUE for a tile, this needs to be rasterized using a finer resolution, for example, using per-pixel resolution. Otherwise the rasterization can be skipped, because the entire tile is either in shadow or lit…" – p. 7, ¶ 86).

11. In regard to claim 10 the rationale disclosed in the rejection of claim 8 is incorporated herein. Aila et al. teach per-pixel processing (p. 5, ¶ 70). It is noted that each of said depth elements 512 are considered to represent respective pixel elements

204 (Greene et al. – Figs. 2, 5A) and therefor the respective teachings of Greene et al. are considered to result, at least in part, in per-pixel processing.

12. In regard to claim 11 Aila et al. teach comparing the stencil code (e.g., shadow information) to a stencil value (the rationale disclosed in the rejection of claim 6 is incorporated herein) and a stencil mask (e.g., shadow information; "…Often information about shadows is called a shadow mask…" – p. 1, ¶ 8; "…There are two alternatives for determining shadows masks, a Z-pass and a Z-fail method…" – p. 1, ¶ 12; "A shadow mask is typically stored in a stencil buffer, and the following description is consistent with this practice…" – p. 3, ¶ 53; "…The minimum and maximum stencil values are also useful for generic computations using stencil buffer…" – p. 8, ¶ 101). It is noted that the respective claim language fails to disclose what exactly constitutes a "stencil code" and a "stencil mask." Thus, a stencil code and stencil mask are considered to read on shadow information.

13. In regard to claim 13 Aila et al. teach wherein said tile Z value range contains a tile (e.g., z_{min}) MinZ and a tile (e.g., z_{max}) MaxZ (the rationale disclosed in the rejection of claim 1 is incorporated herein, specifically: p. 4, ¶ 53). Greene et al. teach wherein said tile Z value range contains a tile (e.g., Z-min) MinZ and a tile (e.g., Z-max) MaxZ and wherein said Z value range contains (e.g., any of the Z-min elements which are covered by such Z-min element in the next finer granularity level) a hierarchical cache MinZ and a (e.g., any of the Z-max elements which are covered by such Z-max element in the next finer granularity level) hierarchical cache MaxZ (the rationale disclosed in the rejection of claim 1 is incorporated herein, specifically: col. 6, ll. 9-36; col. 11, ll. 4-12;

col. 14, ll. 48-67; col. 15, ll. 1-6; col. 17, ll. 24-40). The motivation disclosed in the rejection of claim 8 is incorporated herein.

Response to Arguments

14. In response to Applicant's remarks in regard to "updating" it is noted that the Examiner maintains the position that the respective claim language fails to disclose what exactly constitutes "updating." Thus, it is the position of the Examiner that "updating" is capable of reading on "accessing." Assuming, arguendo, that "updating" is instead read as "changing" said interpretation does not overcome the prior art rejection. The Applicant is directed to the respective above rejection which has been clarified to address Applicant's remarks.

15. Applicant's remarks have been fully considered but they are not persuasive.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PETER-ANTHONY PAPPAS whose telephone number is (571) 272-7646. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Peter-Anthony Pappas/
Primary Examiner, Art Unit 2628